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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/774,685	02/01/2001	Yutaka Yamanaka	1538.1009/JDH	3647

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EXAMINER	
TANG, KUO LIANG J	

ART UNIT	PAPER NUMBER
2122	3

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/774,685	YAMANAKA ET AL.	
	Examiner	Art Unit	
	Kuo-Liang J Tang	2122	

-- Th MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 7-10 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwasawa et al. US Patent No. 5,151,99 (hereinafter Iwasawa).

As Per Claim 1, Iwasawa discloses a parallelization compile method and system which can mitigate the load to users, can parallelize automatically existing serial type programs as such without modification and can generate efficient object codes without taking fine characteristics of hardwares into specific consideration even when coding is made afresh. (See Abstract and FIG. 1 & 2 (storage) and associated text). In that Iwasawa discloses the method that covering the steps of:

"detecting a parallelization directive in said source program;;" (E.g., see FIG. 1, blk 2, and col. 1:59-67 to 2:1-13 which states "...executable parallel processing detected ... "); and

"if said parallelization directive is detected, generating a front-end intermediate language (E.g., see FIG. 1, 3, intermediate language) for said parallelization directive by positioning on a storage region, each processing code of at least part of the parallelization directive with a hierarchical structure(E.g., see FIG. 5) in accordance with an internal structure of said parallelization directive." (E.g., see FIG. 13, PROCESSOR 1 to PROCESSOR NPE).

As Per Claim 2, the rejection of claim 1 is incorporated and further Iwasawa teaches "a step of adding to said front-end intermediate language of a statement to which the parallelization directive is applied, reference information from said front-end intermediate language of said statement to which the parallelization directive is applied, to said front-end intermediate language for the parallelization directive." (E.g., see FIG. 5 & 6 and col. 6:11-27).

As Per Claim 3, the rejection of claim 1 is incorporated and further Iwasawa teaches "a step of, by using a processing table which stores one or a plurality of items of processing information for each of said processing codes, acquiring the processing information corresponding to a current processing content based on said processing code within the front-end intermediate language for said parallelization directive." (E.g., see FIG. 5 & 6 and col. 6:11-27, loop table).

As Per Claim 4, the rejection of claim 3 is incorporated and further Iwasawa teaches "current processing content is one of type analysis, syntactic analysis, semantic analysis, and generation of a compiler intermediate language." (E.g., see FIG. 3, blk 13 (PARSING) & 6 (INTERMEDIATE LANGUAGE) and col. 5:55-67 to 6:1-10).

As Per Claim 7, this is a method version of the claimed storage medium of Claim 1. Thus, the rejection as set forth in Claim 1 also applied.

As Per Claim 13, this is an apparatus version of the claimed storage medium of Claim 1. Thus, the rejection as set forth in Claim 1 also applied.

As per Claims 8-9 and 14-16, recite such claimed limitations which also have been addressed in Claims 2-4, respectively.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5- 6, 11-12 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasawa et al. US Patent No. 5,151,99 (hereinafter Iwasawa) in view of "OpenMP Fortran Application Program Interface", Version 1.1-november-1999 (hereinafter OpenMP).

As Per Claim 5, the rejection of claim 1 is incorporated and further Iwasawa doesn't explicitly disclose said hierarchical structure is a list structure. However, OpenMP teaches "said hierarchical structure is a list structure." (E.g., see pg. 9-11, Section 2.2 Parallel region construct). Iwasawa teaches the parallel execution of each iteration of the loop is detected using FORTRAN language (E.g. see col. 2:19-29), OpenMP teaches a well known FORTRAN structure for Parallel region construct contains such list structure(E.g. PROVATE(list),

SHARE(list) of pg. 9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made incorporate the teaching of OpenMP into the system of Iwasawa, to use a list structure for parallelization detection. The modification would have been obvious because one of ordinary skill in the art would have been motivated use a well known data structure (list) particularly for the same programming language, FORTRAN, to take the advantages of the well known defined structure for the parallelization compile method and system.

As Per Claim 6, the rejection of claim 1 is incorporated and further Iwasawa doesn't explicitly disclose a directive, a clause, and a line, and a processing code for said directive is linked downward to a processing code for said clause, and said processing code for said clause is linked downward to a processing code for said lines.. However, OpenMP teaches "a directive, a clause, and a line, and a processing code for said directive is linked downward to a processing code for said clause, and said processing code for said clause is linked downward to a processing code for said lines." (E.g., see pg. 11-14, Section 2.3.1; pg. 17-18, Section 2.4.1 and pg. 25-29, Section 2.6.2). Iwasawa teaches the parallel execution of each iteration of the (DO) loop is detected using FORTRAN language (E.g. see col. 2:19-29), OpenMP teaches a well known structure for Parallel region construct contains list structure. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made incorporate the teaching of OpenMP into the system of Iwasawa, to use a directive, a clause, and a line, and a processing code. The modification would have been obvious because one of ordinary skill in the art would have been motivated use a well known PARALLEL Do directive (E.g. pg. 17, Section

2.4.1) to take the advantages of the well known defined structure format particularly for the same programming language, FORTRAN, for the parallelization compile method and system.

As per Claims 11-12 and 17-18recite such claimed limitations which also have been addressed in Claims 5-6, respectively.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kuo-Liang J Tang whose telephone number is 703-305-4866. The examiner can normally be reached on M-F 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q Dam can be reached on 703-305-4552.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306.

Kuo-Liang J. Tang

Software Engineer Patent Examiner

TUAN DAM
SUPERVISORY PATENT EXAMINER